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L1	22997	"708"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:16
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L13	6	10 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:20
L14	93	708/620-714.ccls. and (booth adj encoder\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:15
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 Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000  
 IEEE International Symposium on , Volume: 5 , 28-31 May 2000  
 Pages:345 - 348 vol.5

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### 1 Improved design for parallel multiplier based on phase-mode logic

Horima, Y.; Onomi, T.; Kobori, M.; Shimizu, I.; Nakajima, K.;

Applied Superconductivity, IEEE Transactions on , Volume: 13 , Issue: 2 , June 2003

Pages:527 - 530

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### 2 Design and Implementation of a 16 by 16 low-power two's complement multiplier

Goldovsky, A.; Patel, B.; Schulte, M.; Kolagotla, R.; Srinivas, H.; Burns, G.;

Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 5 , 28-31 May 2000

Pages:345 - 348 vol.5

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### 3 Minimizing energy dissipation in high-speed multipliers

Fried, R.;

Low Power Electronics and Design, 1997. Proceedings., 1997 International Symposium on , 18-20 Aug. 1997

Pages:214 - 219

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### 4 An 18 ns 56-bit multiply-adder circuit

Montoye, R.K.; Cook, P.W.; Hokenek, E.; Havreluk, R.P.;

Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th ISSCC., 1990 IEEE International , 14-16 Feb. 1990

Pages:46 - 47, 262

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**1 Modified Booth 1's complement and modulo  $2^n-1$  multipliers***Efstathiou, C.; Vergos, H.T.;*

Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 2 , 17-20 Dec. 2000  
Pages:637 - 640 vol.2

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**2 On the effectiveness of residue code checking for parallel two's complement multipliers***Sparmann, U.; Reddy, S.M.;*

Fault-Tolerant Computing, 1994. FTCS-24. Digest of Papers., Twenty-Fourth International Symposium on , 15-17 June 1994  
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**3 Parallel architecture modified Booth multiplier***Cooper, A.R.;*

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**4 A new architecture for 2's complement Gray encoded array multiplier***Costa, E.; Bampi, S.; Monteiro, J.;*

Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on , 9-14 Sept. 2002  
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**5 A novel redundant binary signed-digit (RBSD) Booth's encoding***Besli, N.; Deshmukh, R.G.;*

SoutheastCon, 2002. Proceedings IEEE , 5-7 April 2002  
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**6 Minimization of switching activities of partial products for designing low-power multipliers**

*Chen, O.T.-C.; Sandy Wang; Yi-Wen Wu;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 11 , Issue: 3 , June 2003

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**7 Two's complement computation sharing multiplier and its applications to high performance DFE**

*Hunsoo Choo; Muhammad, K.; Roy, K.;*

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**8 Approximating elementary functions with symmetric bipartite tables**

*Schulte, M.J.; Stine, J.E.;*

Computers, IEEE Transactions on , Volume: 48 , Issue: 8 , Aug. 1999

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*Sparmann, U.; Reddy, S.M.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 4 , Issue: 2 , June 1996

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**10 A versatile signed array multiplier suitable for VLSI implementation**

*Qi Wang; Shayan, Y.R.;*

Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on , Volume: 1 , 4-7 May 2003

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**11 Low-power multipliers by minimizing inter-data switching activities**

*Sandy Wang; Yi-Wen Wu; Chen, O.T.-C.; Ruey-Liang Ma;*

Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on , Volume: 1 , 8-11 Aug. 2000

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**12 Design and implementation of a 16 by 16 low-power two's complement multiplier**

*Goldovsky, A.; Patel, B.; Schulte, M.; Kolagotla, R.; Srinivas, H.; Burns, G.;*

Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 5 , 28-31 May 2000

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**13 Design of self-timed asynchronous Booth's multiplier**

*Tin-Yau Tang; Chiu-Sing Choy; Pui-Lam Siu; Cheon-Fat Chan;*

Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific , 25-28 Jan. 2000

Pages:15 - 16

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**14 Symmetric bipartite tables for accurate function approximation**

*Schulte, M.J.; Stine, J.E.;*

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**15 A novel approach to the design and hardware implementation of high-speed digit-serial modified-Booth digital multipliers**

*Rao, V.M.; Nowrouzian, B.;*

Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on , Volume: 3 , 9-12 June 1997

Pages:1952 - 1955 vol.3

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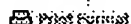
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